4/21/2019 HW12

1. Instruction miss rate: 2%

Data miss rate: 5%

Instruction miss penalty: 100 cycles

Data miss penalty: 200 cycles

CPI: 2

Memory access rate: 30%

Assume run 100 instructions:

Memory access: 100 instructions \* 30% = 30

Data miss: 30 \* 5% = 1.5

Data miss penalty: 1.5 \* 200 = 300 cycles

Instruction miss: 100\*2% = 2

Instruction miss penalty: 200 cycles

Cycles have to run: 2 CPI \* 100 = 200 cycles

Cache improvement ratio: (200+(300+200))/200 = 3.5

1. 